REMARKS

The Applicants respectfully request further examination and consideration in view of the above amendments and the arguments set forth fully below. Claims 1-66 were previously pending in this application. Within the Office Action, Claims 1-13 and 27-49 have been allowed, Claims 14, 19, 20, 25, 26, 50-54 and 60-66 have been rejected, and Claims 15-18, 21-24 and 55-59 have been objected to. By the above amendments, Claims 14 and 50 have been amended. Accordingly, Claims 1-66 are currently pending.

Rejections Under 35 U.S.C. § 102

A. Conley

Claims 50, 60-63 and 65 have been rejected under 35 U.S.C. 102(e) as being anticipated by Conley et al., U.S. Patent No. 6,426,893 (hereinafter "Conley"). Specifically, it is stated within the Office Action that as to claim 50, it is stated that "Conley teaches a flash memory device (fig. 1, el. 17, 11) for storing user data comprising a plurality of separate, independently addressable, independently programmable and independently erasable non-volatile physical memory blocks distinguishably defined by a plurality of physical block addresses (e.g., title, col. 2 line 55 to col. 3, line 10, fig. 12, overhead data blocks and user data blocks) including:

a plurality of dedicated data blocks for storing user data (e.g., fig. 12, user data blocks; col. 2 line 55 to col. 3); and

a plurality of consecutively addressed dedicated overhead blocks for storing overhead data including a first dedicated overhead block and a second dedicated overhead block (e.g., fig. 12, O.H. data blocks; col. 15 line 63 to col. 16, line 65; col. 16, lines 1-17 or fig. 2, fig. 12, reserved, OH data blocks col. 16, lines 60-63; col. 17, lines 8-20); wherein the user data being segregated from the overhead data in separate blocks (e.g., fig. 12, 12, overhead data blocks and user data blocks; col. 2 line 55 to col. 3, line 10)."

The Examiner rejected the Applicants' argument that "Conley failed to teach a flash memory device with a plurality of consecutively address[ed] dedicated overhead blocks." It is further stated in the Office Action that "Conley teaches a plurality of consecutively addressed dedicated overhead blocks for storing overhead data including a first dedicated overhead block and a second dedicated overhead block (e.g., fig. 12, O.H. data blocks col. 16, lines 60-63; col. 17, lines 8-20); wherein the user data being segregated from the overhead data in separate blocks

(e.g., fig. 12, 12, overhead data blocks and user data blocks; col. 2 line 55 to col. 3, line 10)." The Applicants respectfully traverse this rejection.

Conley discloses a flash memory system formed of floating gate memory cells arranged in blocks as the smallest unit of memory cells that are erasable together. One feature of the system is the storage in separate blocks of the characteristics of a large number of blocks of cells in which user data is stored. [Abstract] Conley discloses an example utilization of individual blocks of a memory array chip having **eight units of blocks**, as shown in Fig. 12 and as discussed in col. 16, lines 51-67 and col. 17, lines 1-10. **Within each unit, there is a single overhead data block** (O.H. Data 0 in Unit 0, O.H. Data 1 in Unit 1, ... O.H. Data 7 in Unit 7) followed by a plurality of User Data Blocks. Conley does not teach a plurality of consecutively addressed overhead data blocks. **In fact, Conley teaches away from a plurality of consecutively addressed overhead data blocks because the overhead data blocks are interspersed throughout the memory array, wherein the eight units each have a single overhead data block within the unit.**

In contrast to the teachings of Conley, the method and apparatus of the present invention teaches the segregation of user data, stored in a plurality of dedicated user data blocks, from the overhead data, separately stored in a plurality of dedicated overhead data blocks. Specifically, the overhead data is stored in a plurality of consecutively addressed dedicated overhead blocks, including a first dedicated overhead block and a second dedicated overhead block. Conley does teach a group of blocks devoted to storing overhead data records; however, Conley does not teach that such group of blocks is consecutively addressed. Further, Conley does not teach that overhead data is stored in a plurality of consecutively addressed dedicated overhead blocks, including a first dedicated overhead block and a second dedicated overhead block. Instead, Conley discloses that overhead blocks are interspersed throughout a flash array wherein each unit of the flash array has a single overhead block followed by a plurality of user data blocks. Thus, the overhead blocks disclosed in Conley are not consecutively addressed. **Conley fails to teach a flash memory device with a plurality of consecutively addressed dedicated overhead blocks,** including a first dedicated overhead block and a second dedicated overhead block. In the present invention, the plurality of overhead blocks are consecutively addressed and segregated from the plurality of user blocks within the flash memory array, as depicted in Fig. 7 of the Applicants' patent application.

The independent Claim 50 is directed to a flash memory device for storing user data comprising a plurality of separate, independently addressable, independently programmable and

independently erasable non-volatile physical memory blocks distinguishably defined by a plurality of physical block addresses, including a plurality of dedicated data blocks for storing user data and a plurality of consecutively addressed dedicated overhead blocks for storing overhead data including a first dedicated overhead block and a second dedicated overhead block, wherein the plurality of user data stored in dedicated data blocks is segregated from the plurality of overhead data stored in separate dedicated overhead blocks. As described above, Conley does not teach that overhead data is stored in a plurality of consecutively addressed dedicated overhead blocks, including a first dedicated overhead block and a second dedicated overhead block. In fact, Conley teaches away from a plurality of consecutively addressed overhead data blocks because the overhead data blocks are interspersed throughout the memory array, wherein the eight units each have a single overhead data block within the unit. For at least these reasons, the independent Claim 50 is allowable over the teachings of Conley.

Claims 60-63 and 65 are dependent upon the independent Claim 50. As discussed above, the independent Claim 50 is allowable over the teachings of Conley. Accordingly, Claims 60-63, and 65 also are allowable as being dependent on an allowable base claim.

B. Iida

Claims 14, 19-20, 25, 50-54, 60-63, and 65 have been rejected under 35 U.S.C. 102(e) as being anticipated by Iida et al., U.S. Patent No. 6,625,713 B2 (hereinafter "Iida"). Specifically, it is stated within the Office Action that as to claim 14, Iida teaches "a method of data storage within a flash memory comprising the steps:

Mapping a non volatile memory medium within the flash memory system into a plurality of independently addressable, independently programmable and independently erasable blocks (i.e., segments or blocks, e.g., cols 5-6, figs. 7, 11 and 14) including a plurality of dedicated data blocks (i.e., segments or blocks; e.g., figs. 7A and 11A segments or fig. 7A, blocks n-1 and n; fig. 14B, main data blocks; col. 5 line 55 to col. 6, line 20) and a plurality of dedicated overhead blocks comprising a first dedicated overhead block and a second dedicated overhead block (i.e., segments or blocks; i.e., control data blocks storing overhead data, such as logical address 005, flag 0; figs. 7A and 11A segments or fig. 7A, blocks 0-3; fig. 7F; and col. 5, line 55 to col. 6, line 20; fig. 14C segments or block 123);

Mapping each of the plurality of dedicated overhead blocks into a plurality of consecutive address overhead segments (e.g., figs. 14b-c, pages 0-15) wherein the plurality of segments within each dedicated overhead block are addressed according to an identical set of distinct segment

addresses (e.g., figs. 14b-c, pages 0-15), each segment comprising: physical address register for storing a physical address for locating corresponding user data (e.g., fig. 14 D, 003; col. 12, lines 16-18); and a flag field (e.g., figs. 14 B-C, control flag); and

correlating first group of virtual logical block addresses including a first VLBA to the first dedicated overhead block (e.g., figs 14, redundant portion, logical address); wherein user data and overhead data are in separate blocks (e.g., figs. 14A-D, control data blocks storing overhead data, such as logical address 005, flag 0 wherein the user data, main data, being segregated from the overhead data, logical address 005, flag 0 in separate blocks)." The Applicants respectfully traverse this rejection.

Iida discloses a memory controller for reading data stored in a nonvolatile memory that includes a number of erasable blocks containing a number of pages. A logical/physical address control table stored in a logical/physical address control table block of the nonvolatile memory is searched, read, and manipulated in the nonvolatile memory. [Abstract].

In contrast to the teachings of Iida, the method and apparatus of the present invention teaches the segregation of user data, stored in a plurality of dedicated user data blocks, from the overhead data, separately stored in a plurality of dedicated overhead data blocks, within the flash memory array while maintaining a cross reference between the overhead data and the user data. **The purpose of segregating user data from overhead data is to utilize memory in an efficient manner** when one Logical Block Address repeated more often than another Logical Block Address, or when Logical Block Addresses are used at an equal rate or at variable rates. The present invention discloses a flash memory system maps a non-volatile memory medium into a plurality of independently addressable, independently programmable and independently erasable memory blocks including a plurality of dedicated data blocks and a plurality of dedicated overhead blocks. The dedicated overhead blocks comprise a first dedicated overhead block and a second dedicated overhead block. Each of the dedicated overhead blocks is mapped into a plurality of overhead pages. Each of the overhead pages is mapped into a plurality of overhead segments. The same set of segment addresses is used for each overhead page. Iida does not teach that overhead data is segregated from user data within the flash memory array. Instead, Iida teaches only **partial segregation** of overhead data from user data, only in a portion of the flash memory array (namely, a 4-MB block of the 128-MB capacity flash memory array only) (Figures 13 and 14 and col. 11, lines 33-41). By only segregating part of the overhead data from the user data, Iida discloses **overhead data interspersed with user data** throughout the flash memory array. **In fact, Iida teaches away from a plurality of consecutively addressed overhead data**

blocks segregated from the plurality of user data blocks because the overhead data blocks are interspersed throughout the flash memory array.

The independent Claim 14 is directed to a method of data storage within a flash memory comprising the steps of mapping a non-volatile memory medium within the flash memory into a plurality of independently addressable, independently programmable and independently erasable memory blocks including a plurality of dedicated data blocks and a plurality of dedicated overhead blocks comprising a first dedicated overhead block and a second dedicated overhead block, wherein the plurality of the dedicated data blocks and the plurality of dedicated overhead blocks are segregated; mapping each of the plurality of dedicated overhead blocks into a plurality of consecutively addressed overhead segments, wherein the plurality of segments within each dedicated overhead block are addressed according to an identical set of distinct segment addresses, each segment comprising a physical address register and a flag field; and correlating the first dedicated overhead block to a first group of Virtual Logical Block Addresses including a first Virtual Logical Block Address; wherein user data and overhead data are segregated in separate memory blocks, such that the user data are stored in the plurality of dedicated data blocks and the overhead data are separately stored in the plurality of dedicated overhead blocks. As described above, Iida does not teach that overhead data is segregated from user data within the flash memory array. Iida teaches partial segregation of the overhead data from the user data. Thus, Iida discloses **overhead data interspersed with user data** throughout the flash memory array. **In fact, Iida teaches away from a plurality of consecutively addressed overhead data blocks segregated from the plurality of user data blocks because the overhead data blocks are interspersed throughout the flash memory array.** For at least these reasons, the independent Claim 14 is allowable over the teachings of Iida.

Claims 15-18 and 21-24 are dependent upon the independent Claim 14. As discussed above, the independent Claim 14 is allowable over the teachings of Iida. Accordingly, Claims 15-18 and 21-24 are allowable as being dependent upon an allowable base claim, and are now in condition for allowance.

The independent Claim 50 is directed to a flash memory device for storing user data comprising a plurality of separate, independently addressable, independently programmable and independently erasable non-volatile physical memory blocks distinguishably defined by a plurality of physical block addresses, including a plurality of dedicated data blocks for storing user data and a plurality of consecutively addressed dedicated overhead blocks for storing overhead data including a first dedicated overhead block and a second dedicated overhead block, wherein the

plurality of user data stored in dedicated data blocks is segregated from the plurality of overhead data stored in separate dedicated overhead blocks. As described above, Iida does not teach a flash memory device with a plurality of consecutively addressed dedicated overhead blocks, including a first dedicated overhead block and a second dedicated overhead block, and **Iida also does not teach segregating the plurality of overhead data from the plurality of user data in separate memory blocks in the flash memory array.** For at least these reasons, the independent Claim 50 is allowable over the teachings of Iida

Claims 51-54, 60-63 and 65 are dependent upon the independent Claim 50. As discussed above, the independent Claim 50 is allowable over the teachings of Iida. Accordingly, Claims 51-54, 60-63, and 65 also are allowable as being dependent on an allowable base claim.

Rejection Under 35 U.S.C. § 103

Claim 64 is rejected under 35 U.S.C. 103(a) as being unpatentable over Iida as applied to claim 50 above, and further in view of applicant's admitted prior art, the current specification pages 2-12 and Figs. 1-6 (hereinafter AAPA). The Applicants respectfully disagree.

Claim 64 depends from the independent Claim 50. As discussed above, Claim 50 is allowable over Conley and Iida. Accordingly, Claim 64 is also allowable as being dependent upon an allowable base claim.

Claims 26 and 66 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iida as applied to claims 50 or 14 above, and further in view of Tanaka, U.S. Patent No. 6,466,177 B1 (hereinafter "Tanaka"). The Applicants respectfully disagree.

Tanaka teaches a control method of nonvolatile semiconductor memory including an one time PROM ("OTP") in a part of its memory region, which is capable of writing a mark data reliably preventing erroneous writing, etc. in the OTP region and clearly maintaining the boundary between a written region and a non-written region, and hence reliably storing irreversible changes of state. Tanaka does not teach a flash memory device with a plurality of consecutively addressed dedicated overhead blocks, which is segregated from the plurality of user data blocks. **Accordingly, neither Iida, Tanaka, nor their combination teaches a flash memory device with a plurality of consecutively addressed dedicated overhead blocks, which is segregated from the plurality of overhead data from the plurality of user data in separate memory blocks in the flash memory array.**

Claim 26 depends from the independent Claim 14. As discussed above, Claim 14 is allowable over Iida. Accordingly, Claim 26 is allowable as being dependent upon an allowable base claim.

Claim 66 depends from the independent Claim 50. As discussed above, Claim 50 is allowable over Conley and Iida. Accordingly, Claim 66 is allowable as being dependent upon an allowable base claim.

Claim Objections

Claims 15-18, 21-24, and 55-59 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 15-18 and 21-24 depends from independent Claim 14. Claims 55-59 depends from independent Claim 50. As discussed above, independent Claim14 is allowable over the teachings of Iida and independent Claim 50 is allowable over the teachings of Conley and Iida. Accordingly, Claim 15-18, 21-24, and 55-59 are also allowable as being dependent upon an allowable base claim.

Conclusion

For the reasons given above, Applicant respectfully submit that the Claims 1-66 are in a condition for allowance, and allowance at an early date would be appreciated. Should the Examiner have any questions or comments, the Examiner is encouraged to call the undersigned at (408) 530-9700 to discuss the same so that any outstanding issues can be expeditiously resolved.

Respectfully submitted,
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Dated: 8-26-05

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CERTIFICATE OF MAILING (37 CFR§ 1.8(a))

I hereby certify that this paper (along with any referred to as being attached or enclosed) is being deposited with the U.S. Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to the: Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450

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Date: 8-26-05 By: John D. Owens